Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VDD**
2. **1Y**
3. **1A**
4. **2Y**
5. **2A**
6. **3Y**
7. **3A**
8. **VSS**
9. **4A**
10. **4Y**
11. **5A**
12. **5Y**
13. **6A**
14. **6Y**

**.061”**

**13 12 11 10**

**14**

**1**

**2**

**9**

**8**

**7**

**3 4 5 6**

**MASK**

**REF**

****

**.059”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .04”**

**Backside Potential: VDD or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .059” X .061” DATE: 8/17/21**

**MFG: SILICON SUPPLY THICKNESS .014” P/N: CD4049UB**

**DG 10.1.2**

#### Rev B, 7/19/02